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10/700,183	11/03/2003	Ruben W. Castelino	200310369-1	3977
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HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			EXAMINER KUO, WEINSING W	
			ART UNIT 2826	PAPER NUMBER
			NOTIFICATION DATE 04/08/2008	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM  
mkraft@hp.com  
ipa.mail@hp.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/700,183	<b>Applicant(s)</b> CASTELINO ET AL.
	<b>Examiner</b> W. Wendy Kuo	<b>Art Unit</b> 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 03 November 2003.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) 33 and 34 is/are allowed.

6) Claim(s) 1-32 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 03 November 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/06)  
 Paper No(s)/Mail Date 11/03/2003

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_

5) Notice of Informal Patent Application

6) Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Objections***

1. Claims 6 and 7 are objected to because of the following informalities: claim 11 is directed to a method and not a beacon. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

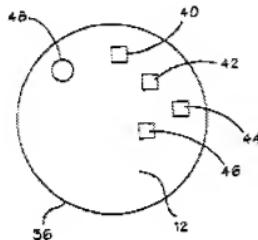
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-4 and 30-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Bethke et al. (US 6,833,718) (hereinafter Bethke).**

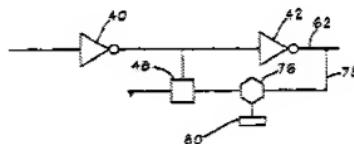
4. With respect to claim 1, Bethke (e.g. Figure 3) teaches a position reference beacon for an integrated circuit, comprising a device 48 capable of emitting radiation (column 5, lines 11-13) and disposed at a reference location on the integrated circuit, wherein the device is capable of being controlled independent of integrated circuit operations (column 5, lines 55-67).

FIG. 3



5. With respect to claim 2, Bethke (e.g. Figure 8) teaches a control circuit 80 connected to the device and configured to selectively enable the device to emit radiation (column 7, lines 10-25).

FIG. 8



6. With respect to claim 3, Bethke teaches that the control circuit is responsive to a signal external to the integrated circuit (column 7, lines 23-25).

7. With respect to claim 4, Bethke teaches that the device is a field-effect transistor (FET) that emits photons when the FET experiences a hot carrier event (column 7, lines 1-9; column 2, lines 52-54).

8. With respect to claim 30, Bethke (e.g. Figure 4) teaches an integrated circuit, comprising at least one beacon circuit (50, 52, 54), each having at least one component capable of emitting radiation and being disabled without impacting normal operation of

the integrated circuit (column5, lines 55-67) and functional circuitry (56, 58) located on the integrated circuit at a predetermined location relative to the at least one beacon circuit.

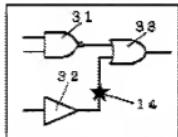
9. With respect to claim 31, Bethke (e.g. Figure 8) teaches a control circuit 80, connected to the at least one beacon circuit, configured to selectively enable at least one beacon circuit (column 7, lines 10-25).

10. With respect to claim 32, Bethke teaches that when the integrated circuit operates in a test mode, a control circuit enables at least one beacon circuit, and when the integrated circuit operates in another mode, the control circuit disables the at least one beacon circuit (column 5, lines 52-57).

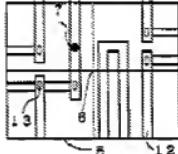
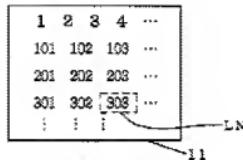
**11. Claims 8-9, 11-21, 23-27, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida (US 6,031,985) (hereinafter Yoshida).**

12. With respect to claim 8, Yoshida (e.g. Figures 3A-3D) teaches a method for identifying a location of interest on an integrated circuit, comprising providing at least one beacon 7 capable of emitting radiation, positioned at a reference location on the integrated circuit (column 5, lines 54-57) and capable of being controlled independent of the normal operation of the integrated circuit (column 9, lines 51-60).

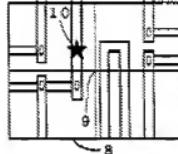
**FIG. 3A**



**FIG. 3B**



CF



**FIG. 3D**

**FIG. 3C**

13. With respect to claim 9, Yoshida teaches that the method further comprises causing one or more of the at least one beacon to emit radiation (column 9, lines 51-60).
14. With respect to claim 11, Yoshida teaches that the method further comprises detecting radiation emitted by at least one of the one or more beacons (column 9, lines 54-56).
15. With respect to claim 12, Yoshida teaches that the method further comprises for at least one beacon that produces detected radiation, identifying the reference location that corresponds to that beacon (column 9, lines 61-67; column 1, lines 59-62).
16. With respect to claims 13-16, Yoshida teaches that the method further comprises (column 1, lines 52-67 – column 2, lines 1-24; column 6, lines 64-67 – column 7, lines 1-10):

- Using at least one identified reference location to identify the location of interest on the integrated circuit;
- Using information about the position of the location of interest, relative to the at least one identified reference location, to identify the location of interest on the integrated circuit;
- Providing the coordinates of the location of interest;
- Providing information about a circuit located at the location of interest

17. With respect to claim 17, Yoshida teaches that the method further comprises using the reference location that corresponds to at least one beacon to register an image window of an integrated circuit diagnostic tool (column 5, lines 60-67 – column 6, lines 1-15).

18. With respect to claim 18, Yoshida teaches that the integrated circuit diagnostic tool is a light emission microscopy system (column 9, lines 45-56).

19. With respect to claim 19, Yoshida (e.g. Figures 3A-3D) teaches a method for identifying a location on an integrated circuit, comprising causing at least one beacon 7 on the integrated circuit to emit radiation (column 9, lines 51-60); and registering information about locations of interest on the integrated circuit with a location of at least one beacon (column 5, lines 47-67; column 6, lines 64-67; column 7, lines 1-10).

20. With respect to claim 20, Yoshida teaches that the method further comprises detecting radiation emitted by at least one of the at least one beacon (column 9, lines 54-56).

21. With respect to claim 21, Yoshida teaches that the method further comprises detecting radiation emitted by circuits of interest in the integrated circuit (column 7, lines 12-22).
22. With respect to claim 23, Yoshida (e.g. Figures 3A-3D) teaches a method for identifying a location on an integrated circuit, comprising causing one or more independently-controllable beacons 7 on the integrated circuit to emit radiation (column 9, lines 51-60); and establishing a frame of reference based on a location the at least one beacon from which radiation is detected (column 5, lines 47-65).
23. With respect to claim 24, Yoshida teaches that the method further comprises detecting radiation emitted by at least one of the beacons (column 9, lines 54-56).
24. With respect to claim 25, Yoshida teaches that the method further comprises detecting radiation emitted by a circuit on the integrated circuit (column 7, lines 12-22).
25. With respect to claim 26, Yoshida teaches that the method further comprises using the frame of reference to identify a location on the integrated circuit that is a source of the radiation emitted by the circuit (column 5, lines 47-67; column 6, lines 64-67; column 7, lines 1-10).
26. With respect to claim 27, Yoshida teaches that the method further comprises using the identified location on the integrated circuit to identify the circuit that emitted the detected radiation (column 7, lines 11-22).
27. With respect to claim 29, Yoshida teaches that the method further comprises using the frame of reference to calculate a position on the integrated circuit of a location

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of interest; and detecting radiation emitted from the calculated position on the integrated circuit (column 6, lines 64-67 - column 7, lines 1-10).

***Claim Rejections - 35 USC § 103***

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

29. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

30. **Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bethke in view of Lieber et al. (US 2003/0089899) (hereinafter Lieber).**

Bethke teaches all of the limitations of claim 1 above.

Bethke fails to teach that the device is a light-emitting diode. Lieber teaches that light-emitting diodes are capable of emitting radiation [0261] because of their suitability for transport of charge carriers [0003].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Bethke with the diode of Lieber for the benefit of enhancing the transport of charge carriers.

**31. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Lieber.**

Yoshida teaches all of the limitations of claim 11 above.

Yoshida fails to teach that the device is a light-emitting diode or a quantum dot. Lieber teaches that light-emitting diodes and quantum dots are capable of emitting radiation [0261] because of their suitability for transport of charge carriers [0003].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the method of Yoshida with the light-emitting diode/quantum dot of Lieber for the benefit of enhancing the transport of charge carriers.

**32. Claims 10, 22, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Bethke.**

33. With respect to claim 10, Yoshida teaches all of the limitations of claim 9 above.

Yoshida fails to teach that wherein the causing one or more of the at least one beacon to emit radiation comprises for each of the one or more of the at least one beacon, applying voltages to a device to increase a likelihood that the device experiences a hot carrier effect. Bethke teaches that wherein the causing one or more of the at least one beacon to emit radiation comprises for each of the one or more of the at least one beacon, applying voltages to a device to increase a likelihood that the

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device experiences a hot carrier effect (column 5, lines 55-67) in order to provide an improved method for fault detection of large scale integrated circuits by decreasing the acquisition time for PICA imaging by increasing photon output (column 5, lines 20-21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the method of Yoshida with the step of Bethke of applying voltages to a device for the benefit of providing an improved method for fault detection of large scale integrated circuits by decreasing the acquisition time for PICA imaging by increasing photon output.

34. With respect to claims 22 and 28, Yoshida teaches all of the limitations of claims 19 and 23, respectively, above.

Yoshida fails to teach causing the one or more beacons to cease emitting radiation. Bethke teaches causing the one or more beacons to cease emitting radiation (column 6, lines 50-51) in order to examine the improvement in photon generation as a function of time (column 6, lines 44-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the method of Yoshida with the step of Bethke of causing the one or more beacons to cease emitting radiation for the benefit of examining the improvement in photon generation as a function of time.

***Allowable Subject Matter***

35. Claims 33-34 are allowed.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. Wendy Kuo whose telephone number is (571)270-1859. The examiner can normally be reached Monday through Friday 7:00 AM to 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached at (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/  
Primary Examiner, Art Unit 2826

W. Wendy Kuo  
Examiner  
Art Unit 2826

WWK